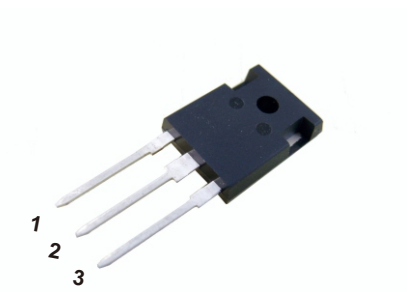
High Efficiency SCRs, 50A/1200V

Main Features

Symbol	Value	Unit
$I_{T(AV)}$	50	A
V_{DRM}/V_{RRM}	1200	V
$I_{GT(Max.)}$	40	mA
$I_{T(RMS)}$, package limit	65	A



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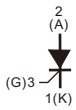
(**non-Insulated**)



DESCRIPTION

The 55PT12C1 series of silicon controlled rectifiers are suitable for general purpose applications, where power handling and power dissipation are critical.

APPLICATIONS

- Line rectifying 50/60Hz
- Switch mode and resonant mode power supplies
- Motor control
- Power converter
- AC power control
- Lighting and temperature control

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	TEST CONDITIONS		VALUE	UNIT
RMS on-state current full sine wave (180° conduction angle)	$I_{T(RMS)}$	T_c=80°C		65	A
Average on-state current (180° conduction angle)	$I_{T(AV)}$	T_c=80°C		50	A
Non repetitive surge peak on-state current (full cycle, T_j initial = 25°C)	I_{TSM}	F =50 Hz	t = 20 ms	600	A
		F =60 Hz	t = 16.7 ms	630	
I^2t Value for fusing	I^2t	t_p = 10 ms		1800	A^2s
Critical rate of rise of on-state current V_D=67% V_{DRM}, t_p=200µs, I_G=0.3A d_{IG}/dt=0.3A/µs	dI/dt	F = 50 Hz, T_j =125°C	I_T = 40A, repetitive	150	A/µs
			I_T = 50A, non-repetitive	500	
Peak gate current	I_{GM}	T_p = 20 µs	T_c =125°C	5	A
Maximum gate power	P_{GM}	T_p = 20 µs	T_c =125°C	10	W
Average gate power dissipation	$P_{G(AV)}$	T_c =125°C		1	W
Repetitive peak off-state voltage	V_{DRM}	T_j =25°C		1200	V
Repetitive peak reverse voltage	V_{RRM}				
Storage temperature range	T_{stg}			- 40 to + 150	°C
Operating junction temperature range	T_j			- 40 to + 125	
Maximum peak reverse gate voltage	V_{RGM}			5	V

ELECTRICAL SPECIFICATIONS (T_J = 25 ºC unless otherwise specified)						
SYMBOL	**PARAMETER**	**TEST CONDITIONS**			**VALUE**	**Unit**
I_{GT}	Gate trigger current	V_D = 12V, R_L = 30Ω		Max.	40	mA
V_{GT}	Gate trigger voltage			Max.	1.5	V
V_{GD}	Gate non-trigger voltage	V_D = 0.67 V_{DRM}	T_j = 125°C	Max.	0.2	V
I_{GD}	Gate non-trigger current				3	mA
I_H	Holding current	I_T = 1A, gate open		Max.	60	mA
I_L	Latching current	I_G = 1.2×I_{GT}		Max.	80	mA
dV/dt	Critical rate of rise of voltage	V_D = 67% V_{DRM}, gate open	T_j = 125°C	Min.	1000	V/μs
V_{TM}	Forward voltage drop	I_T = 100A, t_P = 380μs	T_j = 25°C	Max.	1.6	V
I_{DRM} I_{RRM}	Peak reverse and off-state leakage current	V_D=V_{DRM}, V_R=V_{RRM}	T_j = 25°C	Max.	10	μA
			T_j = 125°C	Max.	5	mA
V_{to}	Threshold voltage	for power loss calculation only	T_j = 125°C	Max.	0.90	V
R_t	Slope resistance		T_j = 125°C	Max.	7.5	mΩ

THERMAL RESISTANCE			
SYMBOL	**Parameter**	**VALUE**	**UNIT**
$R_{th(j-c)}$	Junction to case (DC) (Maximum)	0.25	°C/W
$R_{th(c-h)}$	Case to heatsink (Typical)	0.25	

ORDERING INFORMATION					
ORDERING TYPE	**MARKING**	**PACKAGE**	**WEIGHT**	**BASE Q'TY**	**DELIVERY MODE**
55PT12C1	55PT12C1	TO-247	5g	30	Tube

ORDERING INFORMATION SCHEME

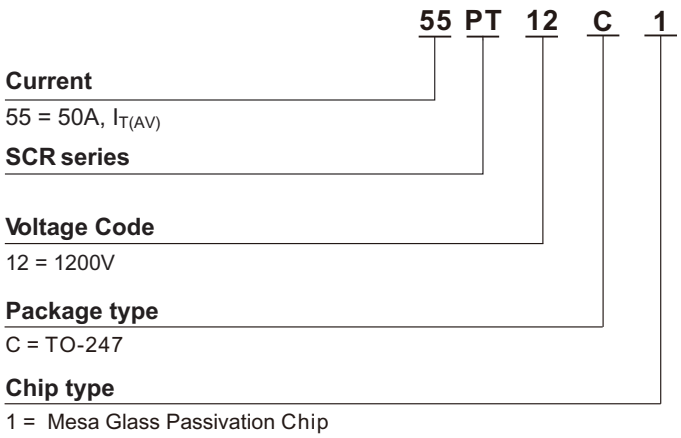


Fig.1 Maximum power dissipation versus average on-state current (half cycle)

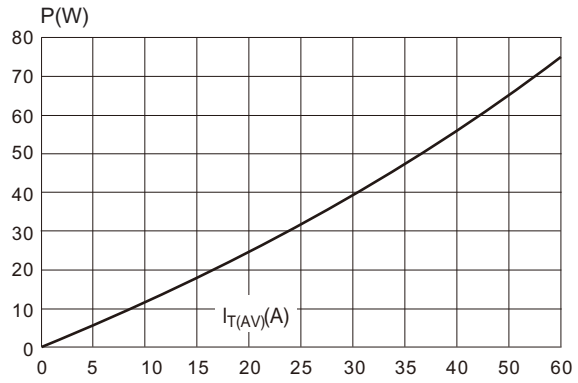


Fig.2 RMS on-state current versus case temperature (full cycle)

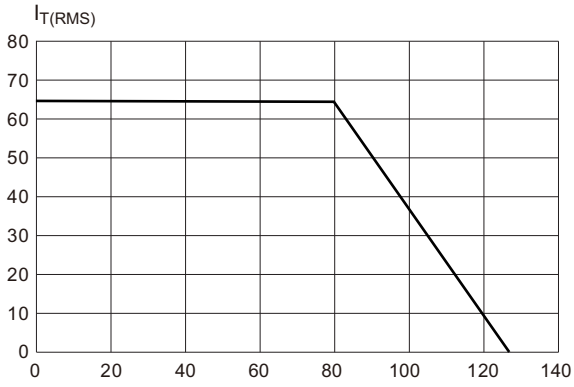


Fig.3 On-state characteristics (maximum values).

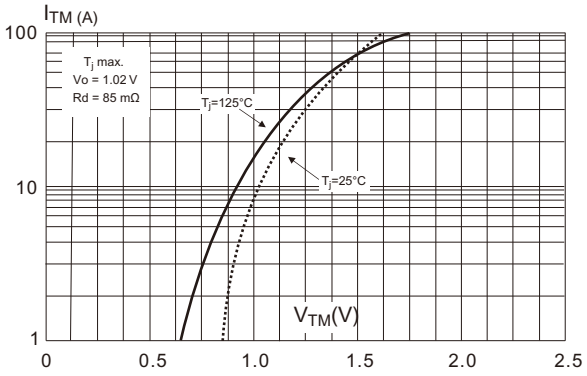


Fig.4 Surge peak on-state current versus number of cycles.

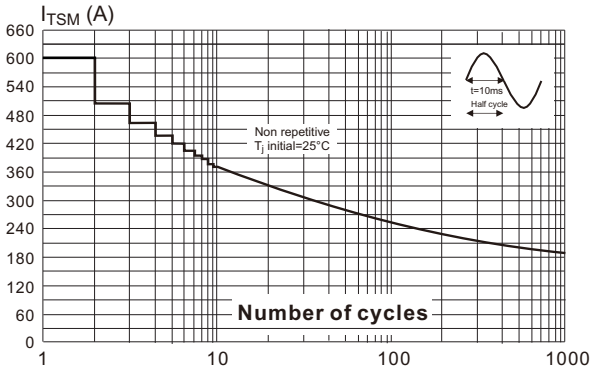


Fig.5 Non-repetitive surge peak on-state current for a sinusoidal pulse with width tp < 10 ms, and corresponding value of I^2t .

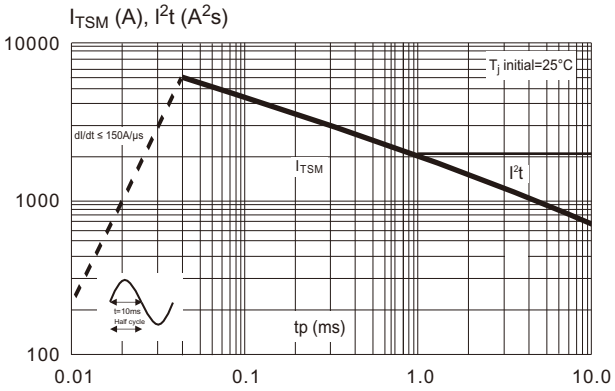
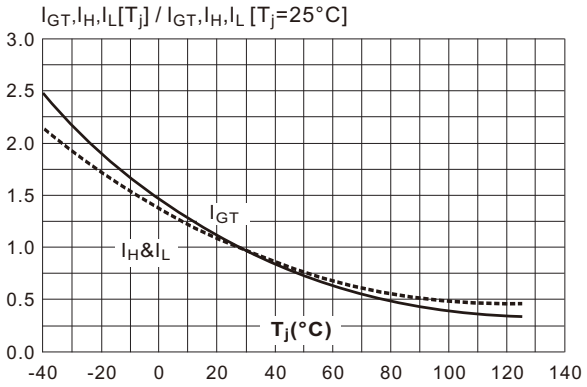


Fig.6 Relative variations of gate trigger current, holding current and latching current versus junction temperature (typical values)



Case Style

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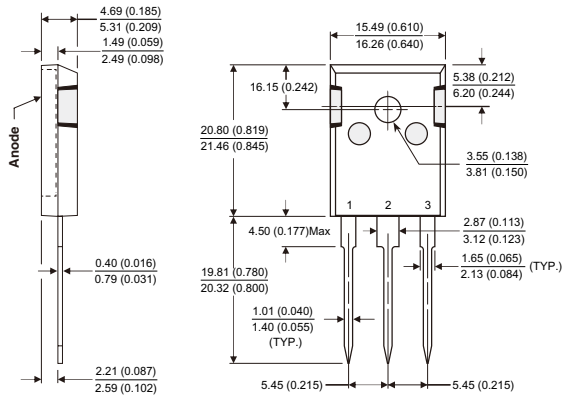

All dimensions in millimeters(inches)